

patentably over the cited prior art for at least the reasons set forth below.

Claims 13-16

Among other things, the capacitors of claims 13-16 include a plurality of groups of vias, **each group corresponding to one of the line pairs and including a plurality of vias directly connecting the first level line and the second level line of the corresponding line pair.**

No such feature is disclosed or suggested by Ng. In Ng Fig. 8, for example, NONE of the plurality of vias 230 **directly connect** a first level line and a second level line of any corresponding line pair. Indeed, as can be more easily seen in FIG. 11, in the device disclosed by Ng, the vias are exclusively provided at the interconnecting electrodes 210, 220, etc. and never directly connect to the first level lines 211 or 221.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 13 is patentable over Ng. Claims 14-16, dependent from claim 13, are deemed patentable for at least the same reasons.

Claim 17

Claim 17 depends from claim 13 and is deemed patentable for at least the reasons set forth above with respect to claim 13 and the following additional reasons.

Among other things, the capacitor of claim 17 includes a plurality of groups of vias, wherein each group includes: a first via directly connecting the first level line and the second level line of the corresponding line pair at respective first ends of the first and second level lines, and a second via directly connecting the first level line and the

second level line of the corresponding line pair at respective second ends of the first and second level lines, wherein the second ends are opposite the first ends along the first direction.

No such feature is disclosed or suggested by Ng.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 17 is patentable over Ng.

Claim 18-20

Among other things, the capacitors of claims 18-20 include a plurality of groups of vias, **each group including a plurality of vias extending directly between the first level line and the second level line of a line pair**. No such feature is disclosed or suggested by Ng. In Ng Fig. 8, for example, NONE of the plurality of vias 230 extend directly between a first level line and a second level line of any line pair. Indeed, as can be more easily seen in FIG. 11, in the device disclosed by Ng, the vias are exclusively provided at the interconnecting electrodes 210, 220, etc. and never extend to any of the first level lines 211 or 221.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 18 is patentable over Ng. Claims 19-20, dependent from claim 18, are deemed patentable for at least the same reasons, and for the following additional reasons.

CONCLUSION

In view of the foregoing explanations, Applicants respectfully request that the Examiner allow claims 1-20 and pass the application to issue. In the event that there


are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (703) 715-0870 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

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Version With Markings to Show Changes Made

In the Claims:

Claim 1 has been amended as follows:

1. (Three Times Amended) A capacitor comprising:

a first level of at least four electrically conductive parallel lines extending in a first direction and lying in a first plane;

at least a second level of at least four electrically conductive parallel lines extending in the first direction and lying in a second plane above the first plane,

each of the second level lines being disposed over a respective one of the first level lines, such that the lines of the first and second levels are arranged in a series of at least four coplanar line pairs, each line pair comprising one of the first level lines and a respective one of the second level lines;

a dielectric layer disposed between the first and second levels of conductive lines;

[an array of vias arranged such that the first level line and the second level line of each of the at least four line pairs is connected by at least a respective plurality of vias, thereby forming an array of at least four parallel capacitor plates]

a plurality of vias arranged in a plurality of groups, each group corresponding uniquely to one of the coplanar line pairs and including at least two vias connecting the first level line and the second level line of the corresponding line pair; and

electrically opposing nodes forming the terminals of the capacitor, the array of

parallel capacitor plates electrically connected to the opposing nodes in an alternating manner so that the plates have alternating electrical polarities.